

AMENDMENT TO CLAIMS

1. (currently amended) An electrically alterable memory device, comprising:
 - a first semiconductor layer doped with a first dopant in a first concentration;
 - a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;
 - two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, and a first channel region defined between the first diffusion region and the second diffusion region;
 - a first floating gate having a first height and comprised of a conductive material, the first floating gate disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the first floating gate capable of storing electrical charge;
 - a second floating gate having a second height and comprised of a conductive material, the second floating gate disposed adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, the second floating gate capable of storing electrical charge; and
 - a control gate having a third height higher than the first height and the second height and comprised of a conductive material, the control gate disposed laterally between the first floating gate and the second floating gate, the control gate separated from the first floating gate by a first vertical insulator layer and separated from the second floating gate by a second vertical insulator layer, the control gate acting as a word select line, the control gate further being above the first channel region without overlapping the two spaced-apart diffusion regions and separated therefrom by a third insulator region.
2. (original) The memory device of claim 1, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

3. (original) The memory device of claim 1, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

4. (original) The memory device of claim 1, wherein the first insulator region having a thickness that allows tunneling of charge between the first floating gate and the first channel region.

5. (original) The memory device of claim 4, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

6. (currently amended) The memory device of claim 1, wherein the ~~third~~ second insulator region having a thickness that allows tunneling of charge between the second floating gate and the first channel region.

7. (previously presented) The memory device of claim 6, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.

8. (original) The memory device of claim 1, wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate and the control gate, and the first vertical insulator preventing leakage between the first floating gate and the control gate.

9. (original) The memory device of claim 1, wherein the first vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the first floating gate and the control gate, and the first vertical insulator prevents leakage between the first floating gate and the control gate.

10. (currently amended) The memory device of claim 1, wherein the ~~first~~ second vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the second floating gate and the control gate, and the ~~first~~

second vertical insulator preventing leakage between the second floating gate and the control gate.

11. (original) The memory device of claim 1, wherein the second vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the second floating gate and the control gate, and the second vertical insulator preventing leakage between the second floating gate and the control gate.

12-14. (canceled)

15. (original) The memory device of claim 1, wherein the first floating gate and the second floating gate each being capable of storing multiple levels of charge.

16. (original) The memory device of claim 1, wherein the first floating gate and the second floating gate each being capable of storing four levels of charge.

17. (original) The memory device of claim 1, wherein an oxidation layer is disposed on top of each diffusion region.

18. (canceled)

19-21. (canceled)

22. (canceled)

23-24. (canceled)

25. (canceled)

26. (canceled)

27-38 (canceled)

39-40. (canceled)

41. (new) An electrically alterable memory device, comprising:

- a first semiconductor layer doped with a first dopant in a first concentration;

- a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

- two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, and a first channel region defined between the first diffusion region and the second diffusion region;

- a first floating gate having a left side, and a right side and comprised of a conductive material, the first floating gate disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the first floating gate capable of storing electrical charge;

- a second floating gate having a left side, and a right side and comprised of a conductive material, the second floating gate disposed adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, the second floating gate capable of storing electrical charge; and

- a control gate comprised of a conductive material, the control gate disposed laterally between the first floating gate and the second floating gate, the control gate separated from the first floating gate by a third insulator layer and separated from the second floating gate by a fourth insulator layer, the control gate covering the first floating gate on at least right side and left side, the control gate further covering the second floating gate on at least right side and left side, the control gate further being above the first channel region and separated therefrom by a third insulator region.

42. (new) The memory device of claim 41, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

43. (new) The memory device of claim 41, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

44. (new) The memory device of claim 41, wherein the first insulator region having a thickness that allows tunneling of charge between the first floating gate and the first channel region.

45. (new) The memory device of claim 44, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

46. (new) The memory device of claim 41, wherein the second insulator region having a thickness that allows tunneling of charge between the second floating gate and the first channel region.

47. (new) The memory device of claim 46, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.

48. (new) The memory device of claim 41, wherein the third insulator is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate and the control gate, and the third insulator preventing leakage between the first floating gate and the control gate.

49. (new) The memory device of claim 41, wherein the third insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the first floating gate and the control gate, and the third insulator prevents leakage between the first floating gate and the control gate.

50. (new) The memory device of claim 41, wherein the fourth insulator is made from a silicon dioxide having a thickness that provides capacitance between the second floating gate and the control gate, and the fourth insulator preventing leakage between the second floating gate and the control gate.

51. (new) The memory device of claim 41, wherein the fourth insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the second floating gate and the control gate, and the fourth insulator preventing leakage between the second floating gate and the control gate.

52. (new) The memory device of claim 41, wherein the first floating gate and the second floating gate each being capable of storing multiple levels of charge.

53. (new) The memory device of claim 41, wherein the first floating gate and the second floating gate each being capable of storing four levels of charge.

54. (new) The memory device of claim 41, wherein an oxidation layer is disposed on top of each diffusion region.

55. (new) An electrically alterable memory device, comprising:

- a first semiconductor layer doped with a first dopant in a first concentration;
- a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;
- two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, and a first channel region defined between the first diffusion region and the second diffusion region;
- a first floating gate comprised of a conductive material, the first floating gate disposed adjacent the first diffusion region and above the first channel region and

separated therefrom by a first insulator region, the first floating gate capable of storing electrical charge;

a second floating gate comprised of a conductive material, the second floating gate disposed adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, the second floating gate capable of storing electrical charge; and

a control gate having at least two lateral sides and comprised of a conductive material, the control gate disposed laterally between the first floating gate and the second floating gate, the control gate separated from the first floating gate by a first vertical insulator layer and separated from the second floating gate by a second vertical insulator layer, the control gate being covered by the first floating gate on more than one lateral side and covered by the second floating gate on more than one lateral side, the control gate being separated from the first channel region by a third insulator region.

56. (new) The memory device of claim 55, wherein the first dopant having a P-type characteristic and the second dopant having an N-type characteristic.

57. (new) The memory device of claim 55, wherein the first dopant having an N-type characteristic and the second dopant having a P-type characteristic.

58. (new) The memory device of claim 55, wherein the first insulator region having a thickness that allows tunneling of charge between the first floating gate and the first channel region.

59. (new) The memory device of claim 58, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

60. (new) The memory device of claim 55, wherein the second insulator region having a thickness that allows tunneling of charge between the second floating gate and the first channel region.

61. (new) The memory device of claim 55, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.
62. (new) The memory device of claim 55, wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate and the control gate, and the first vertical insulator preventing leakage between the first floating gate and the control gate.
63. (new) The memory device of claim 55, wherein the first vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the first floating gate and the control gate, and the first vertical insulator prevents leakage between the first floating gate and the control gate.
64. (new) The memory device of claim 55, wherein the second vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the second floating gate and the control gate, and the second vertical insulator preventing leakage between the second floating gate and the control gate.
65. (new) The memory device of claim 55, wherein the second vertical insulator is made from an oxide nitride oxide having a thickness that provides capacitance between the second floating gate and the control gate, and the second vertical insulator preventing leakage between the second floating gate and the control gate.
66. (new) The memory device of claim 55, wherein the first floating gate and the second floating gate each being capable of storing multiple levels of charge.
67. (new) The memory device of claim 55, wherein the first floating gate and the second floating gate each being capable of storing four levels of charge.

68. (new) The memory device of claim 55, wherein an oxidation layer is disposed on top of each diffusion region.